

FROM  
Intellectual Property Group of  
Pillsbury Winthrop LLP  
Attorneys at Law  
P.O. Box 10500  
McLean, VA 22102

Telephone: (703) 905-2000

Our Facsimile #: (703) 905-2500

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In re PATENT APPLICATION of

Inventor(s) INABA

Appln. No. 10/042,264

series code ↑ serial no.  
Filed: January 11, 2002

Group Art Unit: 2826

Examiner: Dickey, Thomas L.

Atty. Dkt. PM 0284163

TITLE: SEMICONDUCTOR DEVICE AND  
METHOD OF FABRICATING THE  
SAME

Date: April 29, 2004

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REQUEST FOR RECONSIDERATION TRANSMITTAL; REQUEST FOR RECONSIDERATION

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Date April 29, 2004

44020/0284163

C# / M#

Attorney's Docket 044020-0284163  
Client Reference: 01F181

### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of:  
INABA

Confirmation Number: 6258

Application No.: 10/042,264

Group Art Unit: 2826

Filed: January 11, 2002

Examiner: Dickey, Thomas L.

For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

### REQUEST FOR RECONSIDERATION TRANSMITTAL

Transmitted herewith is an amendment/response for this application.

### FEES

The fee for claims and extension of time (37 C.F.R. 1.16 and 1.17) has been calculated as shown below:


	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE		ADDIT. FEE
TOTAL	46	-	46	=	0	x \$ 18.00 =	\$ 0.00
INDEP.	10	-	10	=	0	x \$ 86.00 =	\$ 0.00
FIRST PRESENTATION OF MULTIPLE DEP. CLAIM						+ \$ 290.00 =	\$ 0.00
TOTAL ADDITIONAL CLAIM FEE							\$ 0.00
GRAND TOTAL							\$ 0.00

INABA -- 10/042,264  
Client/Matter: 044020-0284163

**FEE PAYMENT**

Authorization is hereby made to charge the amount of \$0.00 to Deposit Account No. 033975. Charge any additional fees required by this paper or credit any overpayment in the manner authorized above. A duplicate of this paper is attached.

Date: April 29, 2004  
PILLSBURY WINTHROP LLP  
P O. Box 10500  
McLean, VA 22102  
(703) 905-2000  
Customer No.: 00909

  
JOHN P. DARLING  
Reg. No. 44482  
Tel. No.: (703) 905-2045  
Fax No.: (703) 905-2500

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Attorney's Docket 044020-0284163  
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Tel. No.: (703) 905-2045  
Fax No.: (703) 905-2500

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Title: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

REQUEST FOR RECONSIDERATIONCommissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated January 29, 2004, reconsideration in view of the following remarks is respectfully requested.

Claims 1, 4-6 and 11 were rejected under 35 U.S.C. §102(b) over Yazawa et al. (U.S. Patent 4,819,043). The rejection is respectfully traversed.

Claim 1 recites a semiconductor device comprising, *inter alia*, a first impurity doped layer equal to or less in junction depth than the extension region of each of a source/drain diffusion layer. The pair of source and drain diffusion layers are formed in the semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath a gate electrode. Yazawa et al. do not disclose or suggest these features.

Yazawa et al. disclose a MOSFET with reduced short channel effect, otherwise known as a "buried channel device." In such a device, a channel is formed deep inside the substrate, not immediately beneath the gate electrode. In the device of Yazawa et al., a channel is formed in an N-type layer 6 (in the ON state of the MOSFET only), not in the P-type layer 7. (See column 2, lines 20-34 and the cross hatched region of Figure 3b). The N-type layer 6 is sandwiched between the P-type layer 7 and a P-type substrate 1. A gate electrode 3 is formed over the P-type layer 7 via insulating film 2. Accordingly, Yazawa et

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al. do not disclose or suggest a channel formed immediately beneath the gate electrode as recited in claim 1, lines 6-7.

The Office Action on page 3, line 1, alleges that Yazawa et al. disclose a channel region 6-7. However, the P-type layer 7 of Yazawa et al. is not a channel region. The P-type layer 7 of Yazawa et al. is not a channel region as it is of opposite conductivity type to the source/drain layers 4 or 5 and no "diffusion layer" is formed therein, even in the ON state of the MOSFET. (See Figures 3b and 6e.)

The Office Action on page 3, lines 9-8, also alleges that N-type layer 6 of Yazawa et al. is a second impurity layer as recited in claim 1. However, it is respectfully submitted that the N-type layer 6 of Yazawa et al. is not a second impurity layer as recited in claim 1. The N-type layer 6 of Yazawa et al. is depleted only in the OFF state of the MOSFET. In the ON state, the depletion layer is contracted and a channel is formed in the N-type layer 6. Thus, the N-type layer 6 does not provide characteristics similar to that of a fully depleted SOI MOSFET.

Finally, in the device of Yazawa et al., the source and drain diffusion layers 4 and 5 have an extension region. However, the extension regions in Yazawa et al. extend toward the P-type layer 7, in which no channel is formed, and not toward the N-type layer 6, in which the channel is formed.

For the above reasons, it is respectfully submitted that Yazawa et al. do not anticipate claim 1.

Claims 2-11 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 1, and for the additional features recited therein.

Reconsideration and withdrawal of the rejection of claims 1-11 are respectfully requested.

In view of the above remarks, Applicants respectfully submit that all the claims are allowable and that the entire application is in condition for allowance.

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Client/Matter: 044020-0284163

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

PILLSBURY WINTHROP LLP



JOHN P. DARLING

Reg. No. 44482

Tel. No. (703) 905-2045

Fax No. (703) 905-2500

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